



- gating"), contextualizing gating decisions at the lower levels.
- The mid-level level circuit selects context-relevant information from the PFC ("output gating") to guide response selection.
- is appropriate given the output-gated information.

# (modified reference-back task)



- study the mechanisms that underlie input gating.
- In the present study, a category manipulation was added to the task to separately learn about *selective* input and output gating in humans.
- stimulus in each trial was the same as or different from the most recent red stimulus from the same category (letter or symbol).
- Only red trials additionally required WM updating, whereas blue trials required maintenance in WM.





ERP evidence for hierarchical dynamic regulation

ERP at Pz and FCz exhibited respectively, elevated positive and

## EEG correlates of decision dynamics underlying hierarchical working-memory gating

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### Model: hierarchical dynamic regulation of gating decisions

- Each gating decision is accomplished by parallel gating mechanisms. • The "decision threshold" at the response level is raised when there is conflict at higher level frontal representations, allowing decisions to be delayed until cognitive uncertainty is resolved, via the 'hyperdirect pathway' (from mPFC to the STN)[8-9]

Prediction: neural correlates of cognitive conflict adjust decision thresholds during WM gating

### EEG GLM analysis

- A regression approach was used to simultaneously extract the effect of gate switches at all levels on the EEG signal, regressing out RT.
- We identified significant masks (clusters of electrodes and time points) that showed significant sensitivity to each gating decision.
- GLM masks demonstrate mostly parallel processing across levels

### Hierarchical DDM with EEG decoding

- We tested the evidence accumulation processes for selecting correct and incorrect responses during the reference-back task [6-7].
- A similarity index (dot-product) was calculated to generate a trial-by-trial index of associated cognitive process (e.g., how much is the brain in an "response gating" state).
- HDDM [8] was used to test if DDM parameters (threshold and drift-rate) were dynamically modulated by trial-to-trial variations in the EEG similarity index.

### HDDM EEG evidence for hierarchical dynamic regulation Similarity Index

- Terrer Trial level gating conditions Threshold adjustment during output gating by the EEG index of response switch cost maintenance trials 0.150 0.100 0.050 0.000 resp switchina input switchind no other gatin -0.050 output switch output repeat Threshold adjustment during output gating by the EEG index of response switch cost updating trials 0.150 0.100 0.05 0.000 input switchina resp switchina no other gating

output switch = output repeat

-0.050









### Goal

### The aim of this study was to:

- characterize the dynamics that support input, output, and response gating
- identify dynamic interactions that affect decision parameters for action selection

### Summary & Conclusion

- We tested how the decision parameters (threshold and drift rate) are modulated on a trial-to-trial basis by the level of gating conflict.
- Behavior and EEG results suggest that input, output, and response gating mostly operate in parallel [1,2,4,5].
- HDDM EEG regression model showed that the EEG index of response switch cost modulated the output gating threshold. These findings demonstrated that the gating architecture follows a hierarchical top-down influence wherein the engagement of WM updating or output switching can override the motor effects in a top-down way.
- This top-down effect was also demonstrated in the ERP where the response switch activity increased when higher-level processes were *not* involved.
- The finding in FCz electrode is consistent with the idea of a mid-frontal EEG mechanism of cognitive control [11] that regulates the threshold via the mPFC-STN network [7,9] during response conflict.
- Drift rate results (not shown) suggest facilitation when parallel gating circuits are engaged in congruent gating decisions (e.g., response switching and output gate switching).

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### Acknowledgements

We are grateful to Romy Frömer and Matt Nassar for generously sharing code and advice.

This research was supported by THE ISAREL SCIENCE FOUNDATION (grant No. 96/19). And by Fulbright United states – Israel Educational Foundation



United States - Israel Educational Foundation קרן חינוך ארצות הברית - ישראל صندوق التعليم الولايات المتحدة – إسرائيل

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